REMARKS

Applicants respectfully request entry of the following amendments and remarks contained herein in response to the Advisory Action mailed January 8, 2007. Upon entry of this response, claims 1-7, 9-22, and 25 remain pending in the present application. Claims 1-7, 9-22, and 25 are rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by *Bratt* et al. (U.S. Patent No. 6,877,020, hereinafter *"Bratt"*). Applicants have amended independent claims 1, 12 and 18. Reconsideration and allowance of the application and presently pending claims are respectfully requested.

I. Response to Rejections Under 35 U.S.C. § 102(e)

Claims 1-7, 9-22, and 25 stand rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by *Bratt*. It is axiomatic that "[a]nticipation requires the disclosure in a single prior art reference of each element of the claim under consideration." *W. L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 1554, 220 USPQ 303, 313 (Fed. Cir. 1983). Therefore, every claimed feature of the claimed invention must be represented in the applied reference to constitute a proper rejection under 35 U.S.C. § 102(e). For at least the reasons set forth below, Applicants traverse the §102(e) rejections.

Independent Claim 1 is Patentable Over Bratt

Claim 1 stands rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by *Bratt*. Applicants respectfully traverse this rejection and submit that independent claim 1 patently defines over *Bratt* for at least the reason that *Bratt* fails to disclose, teach or suggest certain features in claim 1.

Claim 1, as amended, recites:

> 1. A data converter for converting a group of vectors from a time serial to a time parallel format, wherein in the time serial format, sets of corresponding components of the vectors each have a time slot, and in time parallel format, each vector has a time slot, the converter comprising:
>
> an input rotator configured to rotate each set of corresponding components of all time serial vectors by an amount that depends on the time slot of the set of corresponding components, ***wherein the input rotator is comprised of a plurality of multiplexer stages for rotating the components***;
>
> a bank of register files coupled to the input rotator to receive the rotated set of corresponding components, and having a register file in the bank configured to store each rotated set of corresponding components;
>
> an output rotator coupled to the bank of registers files, for receiving and rotating the components of a vector an amount that depends on the time slot of the vector to generate a vector having time parallel format, ***wherein the output rotator is comprised of a plurality of multiplexer stages for rotating the components***; and
>
> a controller configured to control the addressing of the bank of register files when the corresponding components of each vector are stored in a register of the bank in horizontal and vertical write operations, and to control the addressing of the bank to collect the components of each vector for subsequent output rotation in horizontal and vertical read operations, said controller further configured to control alternating horizontal reading and writing and vertical reading and writing operations upon the bank of register files, ***wherein the controller is comprised of:***
>
> ***address lines configured to identify the proper component register of each respective register bank, wherein the address lines are provided by outputs of multiplexers configured to receive inputs from an up counter and a down counter located within the controller; and***
>
> ***control bits configured to control the operation of the multiplexer stages within the input rotator and the output rotator, wherein the control bits are provided by outputs from the up counter***.

(*Emphasis added.*) Applicants submit that the amendments to claim 1 have been made to clarify certain novel features and that no new matter has been added. Applicants respectfully submit that the *Bratt* reference does not teach the features emphasized in claim 1 (as amended) above. For example, *Bratt* does not teach of an input rotator, "wherein the input rotator is comprised of a plurality of multiplexer stages for rotating the

components," as recited in claim 1 above. The FINAL Office Action (mailed 10/19/06) alleges that "*Bratt* has taught . . . an input rotator *(components that implement operation 9511 as shown in Fig. 75 and described in column 50, lines 56-62)* configured to rotate each set of corresponding components . . ." (*Emphasis added;* Office Action, pg. 2) However, Applicants submit that *Bratt* does not teach of the input rotator being comprised of a plurality of multiplexer stages for rotating the components.

Furthermore, *Bratt* does not teach of a controller comprising "address lines configured to identify the proper component register of each respective register bank, wherein the address lines are provided by outputs of multiplexers configured to receive inputs from an up counter and a down counter located within the controller; and control bits configured to control the operation of the multiplexer stages within the input rotator and the output rotator, wherein the control bits are provided by outputs from the up counter," as recited in claim 1 above. While the Office Action refers to "*components that implement operation . . .* ," there is no mention in the *Bratt* reference of the controller (allegedly the vector processor taught by *Bratt*) having control bits configured to control the multiplexer stages of both the input rotator (allegedly the "components" that implement operation 9511) and the output rotator (allegedly the "components" that implement operation 9515). Nor does the *Bratt* reference teach of an up counter and a down counter located in the controller. Applicants refer the Examiner to the *Bratt* reference, which states that "*FIG. 75 shows methods to transpose a matrix using operations that change the positions of elements . . . . In one embodiment of the present invention, operation 9513 is performed by writing matrix 9532 one row at a time into a vector of look up unit using one set of indices and looking up matrix 9533 one row*

at a time from the vector look up unit using another set of indices." (Col. 50, line 56 to Col. 51, line 3) *Bratt* teaches of using look up tables ("A vector look up units can hold 16 look up tables"; Col. 51, lines 13-14). Accordingly, Applicants submit that independent claim 1 patently defines over *Bratt* for at least the reason that *Bratt* fails to disclose, teach or suggest certain features in claim 1.

Dependent Claims 2-7 and 9-11 are Patentable Over Bratt

Because independent claim 1 patently defines over *Bratt*, dependent claims 2-7 and 9-11 are allowable over *Bratt* as a matter of law for at least the reason that these claims contain all the features and elements of their corresponding independent claim. See, *e.g. In re Fine*, 837 F. 2d 1071 (Fed. Cir. 1988).

Independent Claim 12 is Patentable Over Bratt

Claim 12 stands rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by *Bratt*. Applicants respectfully traverse this rejection and submit that independent claim 12 patently defines over *Bratt* for at least the reason that *Bratt* fails to disclose, teach or suggest certain features in claim 12.

Claim 12, as amended, recites:

> 12. A method for converting a group of vectors from a time serial to a time parallel format, wherein in the time serial format, sets of corresponding components of the vectors each have a time slot, and in time parallel format, each vector has a time slot, the method comprising:
>
> for each set of corresponding components,
>
> rotating the corresponding components an amount that depends on the time slot of the corresponding component, ***wherein the amount is designated by control signals provided by outputs from an up counter located within a controller***;

> writing each set of rotated corresponding components in a separate set of registers in a bank of register files; and
>
> for each vector in the group,
>
> reading selected registers in the bank to collect the components of the vector; and
>
> rotating the collected components of the vector an amount that depends on the time slot of the vector to generate a vector in time parallel format, ***wherein the amount is designated by the same control signals used for rotating each set of corresponding components***;
>
> wherein writing each set of corresponding components and reading the vector components is performed either horizontally or vertically, in an alternating fashion.

(*Emphasis added.*) The Office Action applies the same arguments used in rejecting claim 1 for claim 12. (FINAL Office Action, pg. 6) Applicants have amended independent claim 12, as indicated above, and submit that the amendments were made to clarify certain novel features. No new matter has been added. Applicants respectfully submit that the *Bratt* reference does not teach the features emphasized in claim 12 (as amended) above. Specifically, *Bratt* does not teach the feature wherein the amount of rotation of both the "corresponding components" and "collected components" (from the bank of registers) are controlled by the same control signals. While the Office Action refers to "components that implement operation . . ." in its rejection of claims 1 and 12 (Office Action, pg. 2-3), there is no mention in the *Bratt* reference of control signals that control both of the following: "rotating the corresponding components" and "rotating the collected components" as recited in claim 12 above. Furthermore, the *Bratt* reference does not teach that the control signals are provided by outputs from an up counter located within a controller. Accordingly, Applicants submit that independent claim 12 patently defines over *Bratt* for at least the reason that *Bratt* fails to disclose, teach or suggest certain features in claim 12.

Dependent Claims 13-17 are Patentable Over Bratt

Because independent claim 12 patently defines over *Bratt*, dependent claims 13-17 are allowable over *Bratt* as a matter of law for at least the reason that these claims contain all the features and elements of their corresponding independent claim. See, *e.g. In re Fine*, 837 F. 2d 1071 (Fed. Cir. 1988).

Independent Claim 18 is Patentable Over Bratt

Claim 18 stands rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by *Bratt*. Applicants respectfully traverse this rejection and submit that independent claim 18 patently defines over *Bratt* for at least the reason that *Bratt* fails to disclose, teach or suggest certain features in claim 18.

Claim 18, as amended, recites:

> 18. A data converter for converting a group of vectors from a time serial to a time parallel format, wherein in the time serial format, sets of corresponding components of the vectors each have a time slot, and in time parallel format, each vector has a time slot, the converter comprising:
>
> input rotation means for rotating each set of corresponding components of all vectors by a first prescribed amount depending on the particular set, ***wherein the input rotation means is comprised of a plurality of multiplexing means for rotating the corresponding components***;
>
> storage means coupled to the input rotation means, for storing the rotated set of corresponding components; and
>
> output rotation means coupled to the storage means, for receiving components of a vector from the storage means and rotating the components of the vector by a second prescribed amount depending on the particular vector to generate a vector in time parallel format, ***wherein the output rotation means is comprised of a plurality of multiplexing means for rotating the corresponding components***; and
>
> controller means, communicably coupled to the input rotator means, the storage means and the output rotator means, for controlling the writing and reading of the vector components to the storage means and the rotation of the vector components by the output rotation means and the input rotation means, and for controlling said reading and writing

> operations horizontally and vertically, said horizontal operations alternating with said vertical operations, wherein the input rotator means and the output rotator means are communicably coupled to the controller means through control signals, ***wherein the control signals between the controller and input rotator means are the same control signals between the controller and the output rotator means, and wherein the controller means is comprised of:***
>
> ***address lines configured to identify the proper component register of each respective register bank, wherein the address lines are provided by outputs of multiplexers configured to receive inputs from an up counter and a down counter located within the controller; and***
>
> ***control bits configured to control the operation of the multiplexer stages within the input rotator and the output rotator, wherein the control bits are provided by outputs from the up counter.***

(*Emphasis added.*) The Office Action again applies the same arguments used in rejecting claim 1 for claim 18. (FINAL Office Action, pg. 8) Applicants have amended independent claim 18, as indicated above and submit that no new matter has been added. Applicants respectfully submit that the *Bratt* reference does not teach the features emphasized in claim 18 (as amended) above. The features emphasized above reflect that the control signals coupled between the "control means" and the "input rotation means" are the same control signals coupled between the "control means" and the "output rotation means." (*See, e.g.,* FIG. 3 within the specification.) Applicants submit that this feature is not taught by the *Bratt* reference.

Furthermore, Applicants submit that *Bratt* does not teach that the controller means is comprised of: "address lines configured to identify the proper component register of each respective register bank, wherein the address lines are provided by outputs of multiplexers configured to receive inputs from an up counter and a down counter located within the controller; and control bits configured to control the operation of the multiplexer stages within the input rotator and the output rotator, wherein the

control bits are provided by outputs from the up counter." Accordingly, Applicants submit that independent claim 18 patently defines over *Bratt* for at least the reason that *Bratt* fails to disclose, teach or suggest certain features in claim 18.

Dependent Claims 19-22 and 25 are Patentable Over Bratt

Applicants respectfully submit that because independent claim 18 patently defines over *Bratt*, dependent claims 19-22 and 25 are allowable over *Bratt* as a matter of law for at least the reason that these claims contain all the features and elements of their corresponding independent claim. See, *e.g. In re Fine*, 837 F. 2d 1071 (Fed. Cir. 1988).

CONCLUSION

Applicants respectfully submit that all pending claims are in condition for allowance. Favorable reconsideration and allowance of the present application and all pending claims are hereby courteously requested. If, in the opinion of the Examiner, a telephone conference would expedite the examination of this matter, the Examiner is invited to call the undersigned attorney at (770) 933-9500.

No fee is believed to be due in connection with this response to Office Action. If, however, any fee is believed to be due, you are hereby authorized to charge any such fee to deposit account No. 20-0778.

Respectfully submitted,

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